Lab 10

Single Cycle MIPS Datapath

(R-type and Load/Store)

* Pre-Lab

1. Previous Lab Task

In the last lab you have already implemented Figure 11.1

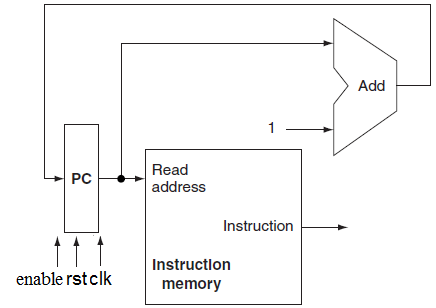


Figure 10.1

1. Today’s Task

In this lab you will create a submodules required for **getoperand module** (enclosed by green box in Figure 10.2.

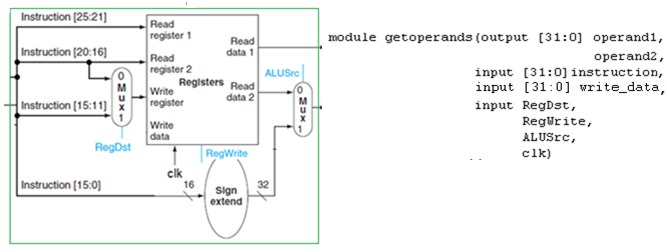


Figure 10.2

* In-Lab

Write Verilog description of these modules separately and test each.

* 1. Composition of module getoperands

It contains,

* + 1. Two 2-1 Muxes

Mux1 has 4-bit inputs/output while mux2 has 32-bit inputs/output.

* + For Mux1

if RegDst==0

muxout=instruction[20:16]

else if RegDst==1

muxout=instruction[15:11]

* + For Mux2

if ALUSrc==0

muxout=ReadData2

else if ALUSrc==1

muxout=outputofsignextender

* + 1. Sign Extender

Sign Extends 16-bit input to 32-bit output such that

If MSB=0 🡪 append 16 zeros at left of the input

If MSB=1 🡪 append 16 ones at left of the input

* + 1. Register File

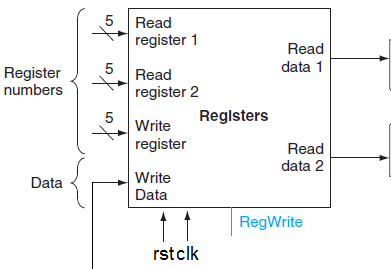
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Figure 11.3

It’s description will be similar to that of instruction memory written in previous lab except that it has two address inputs and two data outputs.

It has 32 registers each 32-bit wide. It has two 32-bit outputs as compared to just one in case of instruction memory. That’s why it has two 5-bit address inputs ‘Read register1’ and ‘Read register 2’. Another 5-bit address input is for destination register, ‘Write register’, where calculation result is written.

Read data 1=Register[Read Register1]

Read data 2=Register[Read Register2]

Register[Write Register]=Write Data

* Post-Lab

All modules separately tested

**Submission details**

* **Your lab report, a .doc file, should contain properly commented Post-Lab task code, with Screenshots(of print preview) of Schematic and waveforms, and Critical Analysis.**
* **The report must have a title page in the pescribed format.**
* **Name the .doc file RegNo.docx; eg SP14-BCE-99.docx**
* **Sumbit on portal.**